Comparison Sheet

Between W5100 and W5300

Version 1.0

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Document History Information

Version	Date	Descriptions
Ver. 0.9	Mar. 11, 2008	Release with W5300 launching
Ver. 1.0	May, 15, 2008	◦ Replace W5300 image on front page. ◦ Modify the phase “Register >> Expansion”, Refer to P.4 Modify the <Note 1> description ◦ Add Sn_DPORTR description to the phase “Register >> Expansion”, Refer to P.4. Add <Note 2>

W5100 vs W5300

As W5300 is based on TCP/IP Core of W5100, it follows basic functions of W5100. One of the main differences between W5100 and W5300 is the data bus. W5100 supports 8bit data bus, but W5300 does not only 8 bit but also 16 bit data bus. With this data bus expansion, the registers of W5300 are also based on 16 bit.

■ Host Interface

	W5100	W5300
Address Bus	15 PINs, ADDR[14:0]	10PINs, ADDR[9:0]
Data Bus	Only 8 Bit, DATA[7:0]	16/8 Bit, DATA[15:8]/DATA[7:0]
Interface Mode	Direct/Indirect, SPI	Direct/Indirect
Interface Timing	No configuration	Partially Configurable [1]
Interrupt PIN(/INT)	No configuration of next assert time	Configurable next assert time [2]
Buffer Ready PIN (BRDY[3:0])	None	Monitoring the buffer Depth of selected SOCKET.

<Note> 1. By setting MR of W5300, the Fetch Timing of Host-Write-Data or Hold Timing of Host-Read-Data can be configurable.

2. Interrupt assert time can be controllable at the W5300. With this function, the interrupt can be processed without a hitch even in the low-level MCU.

■ Network Interface

	W5100	W5300
Link LED(LINKLED)	Blink	No Blink (Hold Low)
External MII	No	MII_TXEN, MII_TXD[3:0], MII_TXC, MII_CRS, MII_COL, MII_RXDV, MII_RXD[3:0] [1]

<Note> 1. MII_TXEN and MII_TXD[3:0] are Alternate Function PINs to be used for Network Indicator LED signal. This PINs are used for MII signals according to TEST_MODE[3:0] PIN Configuration. As W5300 supports MII signals, the PHY chips from 3rd party can be interfaced instead of using the PHY embedded in W5300.

■ Register

The registers of W5300 are almost same as W5100. The differences in register usage are as below.

▪ Expansion

	W5100	W5300
MR	1 Byte	2 Bytes Host I/F Timing and FIFO swap are added
TMSR	1 Byte (2bit per SOCKET)	2 Bytes X 4 (1 Byte per SOCKET)
RMSR	1 Byte (2 bit per SOCKET)	2 Bytes X 4 (1 Byte per SOCKET)
Sn_MR	1 Byte	2 Bytes TCP Alignment Bit is added
Sn_TX_FSR	2 Bytes	4 Bytes
Sn_RX_RSR	2 Bytes	4 Bytes
PSIDR [1]	Use S0_DPORTR [2]	S0_DPORTR [2] & PSIDR
PDHAR [1]	Use S0_DHAR	S0_DHAR & PHAR

<Note> 1. Session ID and PPPoE server hardware address are used for PPPoE mode. At the W5100, Session ID and PPPoE server hardware address can be gotten or set through S0_DPORTR and S0_DHAR which are supported both Host-Read and Host-Write. But at the W5300, Session ID and PPPoE server hardware address can be gotten only through PSIDR and PDHAR, and can be set through S0_DPORTR and Sn_DHAR such as W5100.

2. At the W5100, Sn_DPORTR supports both Host-Read and Host-Write. But, At the W5300, Sn_DPORTR supports only Host-Write.

▪ Addition

ICFGR	Set the Next Interrupt assert time
MTYPER	Set the Internal memory block Type(TX/RX)
FMTUR	Process the ICMP(Fragment MTU) Packet
Pn_BRDYR	Set the BRDYn PIN
Pn_DPTHR	SOCKET n Buffer Depth Monitoring
IDR	W5300 Identification
Sn_IMR	SOCKET n Interrupt MASK
Sn_KPALVTR	TCP Keep-Alive Timer
Sn_TX_WRSR	Write Size of TX memory

Sn_FRAGR	Configure the fragment field in IP Header
Sn_TX_FIFOR	The only access to TX memory
Sn_RX_FIFOR	The only access to RX memory

- Removal

Sn_TX_RD	Only use in W5100.
Sn_TX_WR	
Sn_RX_RD	

■ Memory for data communication

	W5100	W5300
Access	Directly addressing	Only through Sn_TX_FIFOR/Sn_RX_FIFOR
Size	Fixed Size. Total 16KBytes TX : 8KBytes, RX : 8Kbytes	Configurable [1]. Total 128KBytes TX : 0~128KBytes, RX : 0~128KBytes
Manipulation	Calculate the Pointer Registers (Sn_TX_RD,Sn_TX_WR,Sn_RX_RD)	No Calculation No exist the pointer Register.

<Note> 1. The internal memory of W5300 is configurable for TX and RX buffer in the range of 128Kbyte by using TSMR, RMSR, and MTYPER. The TX/RX buffer size should be set as the value, multiple of 8. According to the size, each bit of MTYPER is configurable.

■ SOCKET

	W5100	W5300
Count	4	8
TX memory	Allocable 1/2/4/8 KBytes	Allocable from 0 to 64Kbytes [1]
RX memory	Allocable 1/2/4/8 KBytes	Allocable from 0 to 64Kbytes [1]

<Note> 1. TX/RX memory of each socket can be set as the value ranged from 0Kbytes to 64Kbytes through TMSRn and RMSRn.

■ Data Transmit Size

	W5100	W5300
Transmit Size	No need	Need to set transmit size to Sn_TX_WRSR

At the W5100, the host calculates and updates memory related Pointer Registers (Sn_TX_RD,

Sn_TX_WR), and access the memory in Byte unit. Therefore it is possible to get the information of real TX data size by using Sn_TX_RD and Sn_TX_WR.
W5300 does not have those Pointer Register, and memory access can be done in Word(2 Bytes) unit. Therefore, real TX data size should be set in the Sn_TX_WRSR.

■ Check Data Reception

	W5100	W5300
Check RX	Interrupt(Sn_IR(RECV)) Received Size(Sn_RX_RSR)	Interrupt(Sn_IR(RECV)) Received Size(Sn_RX_RSR) BRDYn PINs [1]

<Note> 1. W5300 checks data reception in the same method of W5100. In addition, W5300 supports 4 BRDYn PINs to monitor the Buffer Depth of SOCKET n. BRDYn can select SOCKET Num, Signal Polarity and Memory Type (TX/RX), and is assert when the Buffer Depth of SOCKET n is same as or bigger than the value of Pn_BDPTHR. The host could monitor the BRDYn PIN through I/O port or Interrupt PIN.

■ TCP

	W5100	W5300
PACKET-INFO (Header)	No Header	PACKET-INFO addition when Sn_MR(ALIGN) = '0' [1]
Keep-Alive	Manually 1 Byte Keep-alive data	Manually, Automatically [2] 0 byte Keep-alive data

<Note> 1. As memory operation of W5100 is processed in Byte unit, the additional information is not required for Received Data in TCP. However, the memory operation of W5300 is processed in Word(2 Bytes) unit, it is not possible to tell the difference between odd and even number sized TCP data. When receiving the data, Host should analyze the Packet-Info and process the data as big as receive size. If RX data size is in even number, by setting the ALIGN bit of Sn_MR as '1', the PACKET-INFO does not need to be added.

2. According to the setting value of Wn_KPALVTR, W5300 can transmit Keep Alive Packet of 0 Byte Data size manually (Sn_KPALVTR=0x00 and SEND_KEEP command) or automatically (Sn_KPALVTR > 0 and without command)

■ MACRAW

	W5100	W5300
PACKET-INFO (Header)	Header Size information includes not only Data size but also Header size, 2Bytes.	The Size information of PACKET-INFO just includes Data size.
Received Data Format	Header(2Bytes) + Data	PAKCET-INFO(2Bytes) + DATA packet + CRC(4bytes) [1]
PAUSE FRAME [2]	No support	When receiving PAUSE FRAME from Switch or Router, all data transmission is paused during Pause Time.

<Note> 1. Whenever receiving MACRAW Data at the W5300, CRC(4bytes) data is added lastly. Received CRC is the CRC value of Ethernet Frame, but not used practically. After reading this CRC, the host should ignore it.

2. PAUSE FRAME is the mechanism for data Flow Control among Ethernet network devices. Ethernet Flow Control occurs when the transmission speed of the sender is faster than receiver. In this case, the receiver transmits the PAUSE FRAME to the sender to hold the data transmission for the specified time.

■ Package

	W5100	W5300
Package	64 LQFP	100 LQFP